UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,128	02/13/2004	Till Schloesser	INF-135	3801

48154 7590 07/20/2005

SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
HUYNH, ANDY	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,128	SCHLOESSER ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *20-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,10 and 17-19* is/are rejected.

7)☒ Claim(s) *7-9 and 11-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction Requirement dated May 31, 2005, Applicant has elected Invention I (Claims **1-19**), drawn to a device is acknowledged. Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Accordingly, Claims **20-33** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims **20-33**, drawn to a method.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in GERMANY, 103 06 281.5 on 02/14/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 08/13/2004. The references cited on the PTOL 1449 form have been considered.

Claim Objections

Claim **1** is objected to because of the following reasons.

Line 8, "wherein the active regions ..." should read –wherein active regions ...--.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1-6, 10 and 17-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Figure 1 Prior Art, Applicant's admitted prior art (AAPA) in view of Hofmann (US Pub. No. 2001/0032991 A1 filed 03/28/2001, publication date: 10/25/2001).

Regarding claims **1 and 6**, Figure 1 Prior Art discloses and the corresponding texts as set forth in Background of the Invention, paragraphs [0002]-[0009], a vertical transistor architecture comprises:

an array of vertical transistor cells 81 formed in a substrate 1 and arranged in a transistor plane, in rows in an x direction, and in columns in a y direction perpendicular to the x direction;

an array of active trenches 5, wherein the active trenches separate the rows of transistor cells; and

an array of isolation trenches 6, wherein the isolation trenches separate the columns of transistor cells;

wherein the active regions 3 at least of transistor cells are electrically without connection.

Figure 1 Prior Art fails to teach active regions at least of transistor cells which are adjacent to one another in the x direction are connected to one another, whereby a charge carrier transport is made possible between the active regions of transistor cells which are adjacent in the x direction; wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction. Hofmann teaches in Figs. 4-5 and the corresponding texts as set forth in paragraphs [0048]-[0049] that a memory cell array comprises active regions 3, 4 at least of transistor cells which are adjacent to one another in the x direction are connected to one another via conductive layer 27, whereby a charge carrier transport is made possible between the active regions of transistor cells which are adjacent in the x direction; wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of a memory cell array comprises active regions at least of transistor cells which are adjacent to one another in the x direction are connected to one another via conductive layer 27, whereby a charge carrier transport is made possible between the active regions of transistor cells which are adjacent in the x direction, wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells

that are adjacent to one another at least in the x direction, as taught by Hofmann to incorporate into and modify Figure 1 Prior Art to arrive the claimed limitations the vertical transistor comprising the active regions of transistor cells which are adjacent to one another in the x direction are connected to one another via conductive layer, wherein the active regions are in each case sections of a contiguous layer body, wherein the contiguous body is patterned at least by the isolation trenches in an upper region, and wherein the contiguous body in a lower region connects the active regions of transistor cells that are adjacent to one another at least in the x direction in order to allow charge carriers which would be accumulated in the active/channel regions flow away through the conductive layer.

Regarding claim **2**, Figure 1 Prior Art discloses the vertical transistor cells comprise: respective lower source/drain connection region 2; respective upper source/drain connection regions arranged above the lower source drain regions 4; respective conductive channels 3 disposed between the upper and lower source/drain connection regions; and respective gate electrodes 52 insulated from the active regions by a gate dielectric 51.

Regarding claim **3**, Figure 1 Prior Art discloses the gate electrodes are arranged in the active trenches and wherein the gate electrodes of transistor cells which are adjacent in the x direction are connected to one another and form sections of word lines 521, 522.

Regarding claim **4**, Figure 1 Prior Art discloses the lower source/drain connection regions are in each case connected to a contiguous connection plate 21.

Regarding claim **5**, Figure 1 Prior Art discloses the lower source/drain connection regions are in each case sections of a connection plate 21 that is patterned at least in an upper region and is contiguous in a lower region.

Regarding claim **10**, Figure 1 Prior Art discloses the layer bodies are connected to a structure having a substrate potential.

Regarding claims **17-19**, Figure 1 Prior Art discloses and the corresponding texts as set forth in Background of the Invention, paragraphs [0002]-[0009], the active regions of the transistor cells have a cross-sectional area of essentially F^2 relative to a production-dictated minimum feature size F parallel to the transistor plane, and wherein the area requirement of a transistor cell is essentially 4 F^2; a storage capacitor electrically connected to a source/drain connection region of each selection transistor, whereby an array of memory cells each containing a vertical selection transistor is formed; wherein the selection transistors are connected to the assigned storage capacitor in each case at an upper source/drain connection region.

Allowable Subject Matter

Claims **7-9 and 11-16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art of record, taken alone or in combination, fails to teach or suggest the vertical transistor architecture further comprises a plurality of layer bodies deposed in the transistor cell array and in each case separated from one another by the active trenches as recited in Claim **7**; the vertical transistor architecture wherein the connection plate is patterned in an upper region by the active trenches extending along the x axis, wherein the lower source/drain connection regions are formed in the upper region of the connection plate in each case below the active regions, wherein the isolation

trenches have a smaller depth than the active trenches, and wherein the layer bodies are formed contiguously row by row in each case in a lower region below the isolation trenches as recited in Claim **11**; the vertical transistor architecture wherein the lower source/drain connection regions are formed in each case in an upper region of the connection plate below the active trenches as recited in Claim **13**; the vertical transistor architecture wherein the active regions of transistor cells which are adjacent in the x direction and the y direction are formed contiguously by a single layer body which is patterned by the lower source/drain connection regions as recited in Claim **14**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

07/18/05

Andy Huynh

Patent Examiner